Advanced Analog Integrated Circuits

Operational Transconductance Amplifier III

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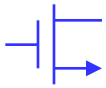
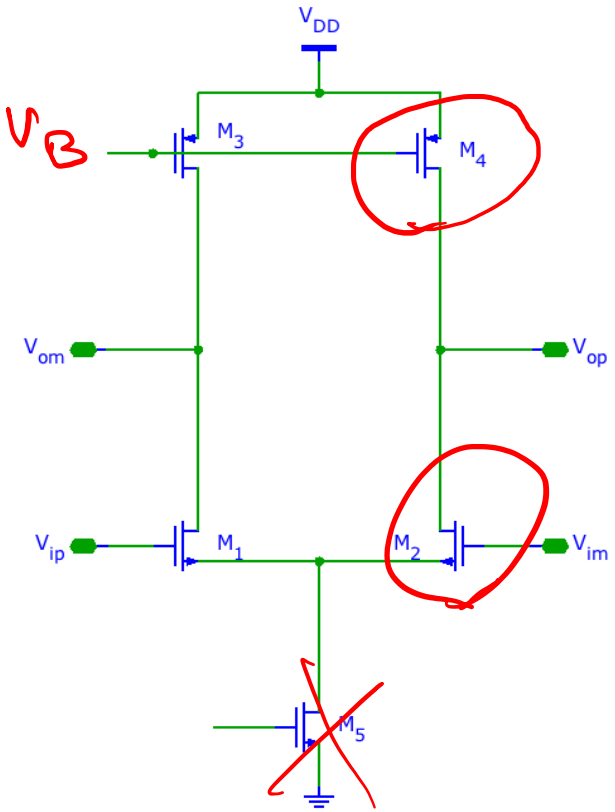


Telescopic OTA

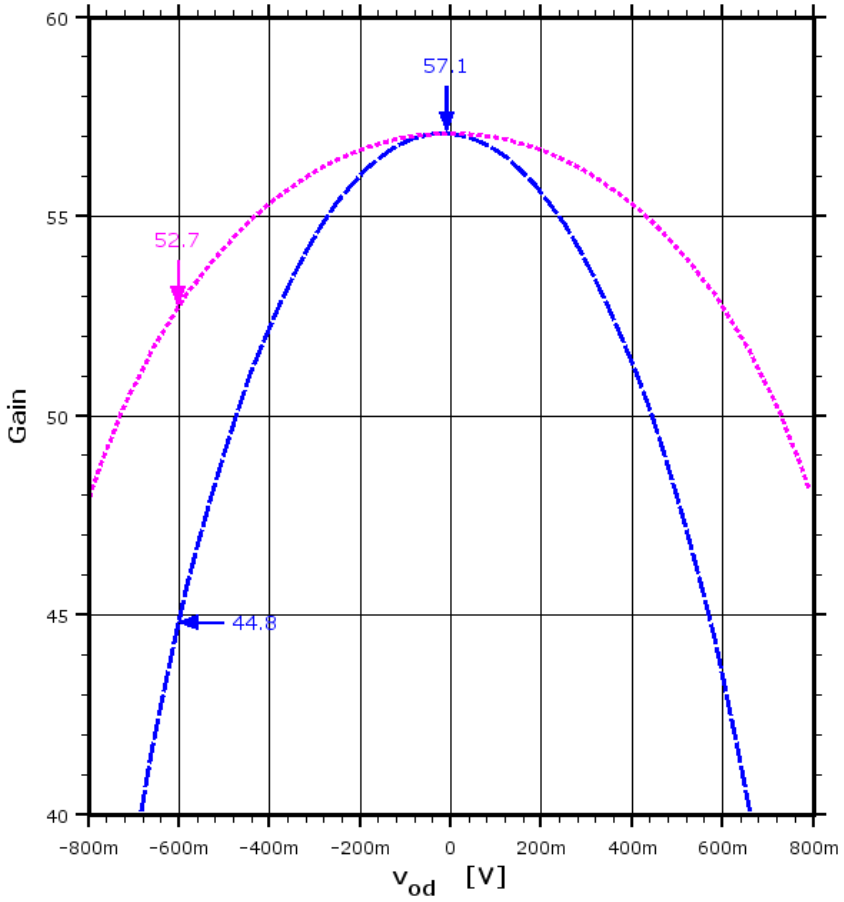


- Simple
- Low power !

$$\alpha = 1 + \frac{V^*_{GS2}}{V^*_{f}}$$

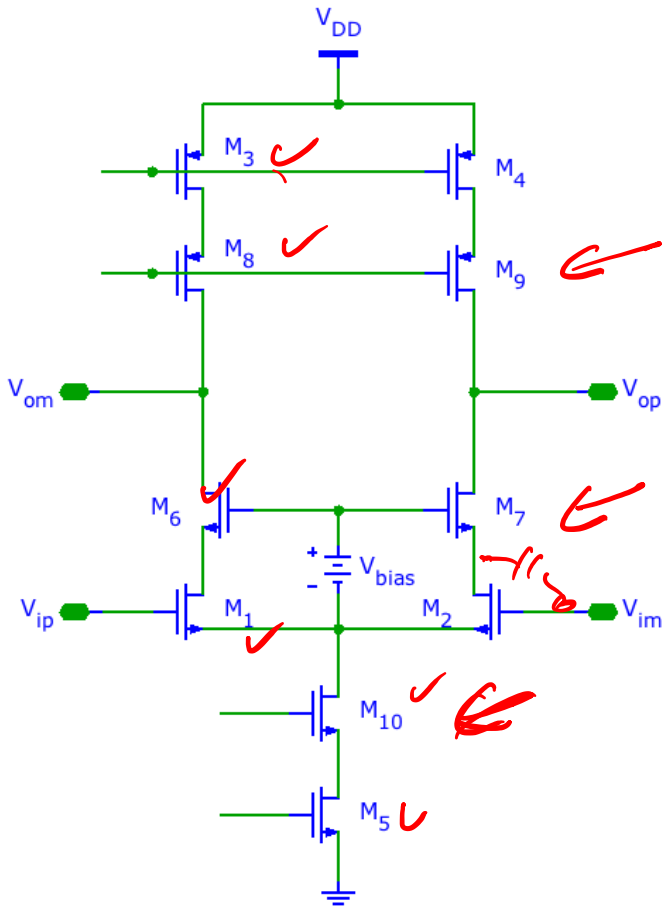
$$\approx 2$$

Output Swing versus Gain



- minimum gain matters
- $R_o = R_{on} \parallel R_{op}$

Cascoded Telescopic OTA



+ CMRR, PSRR

+ small power

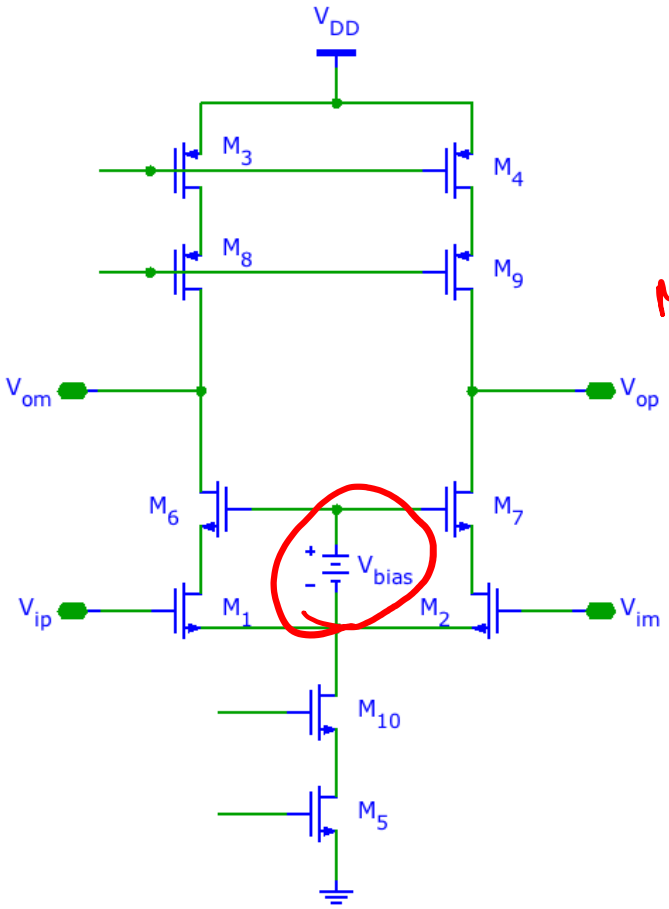
+ ~same noise

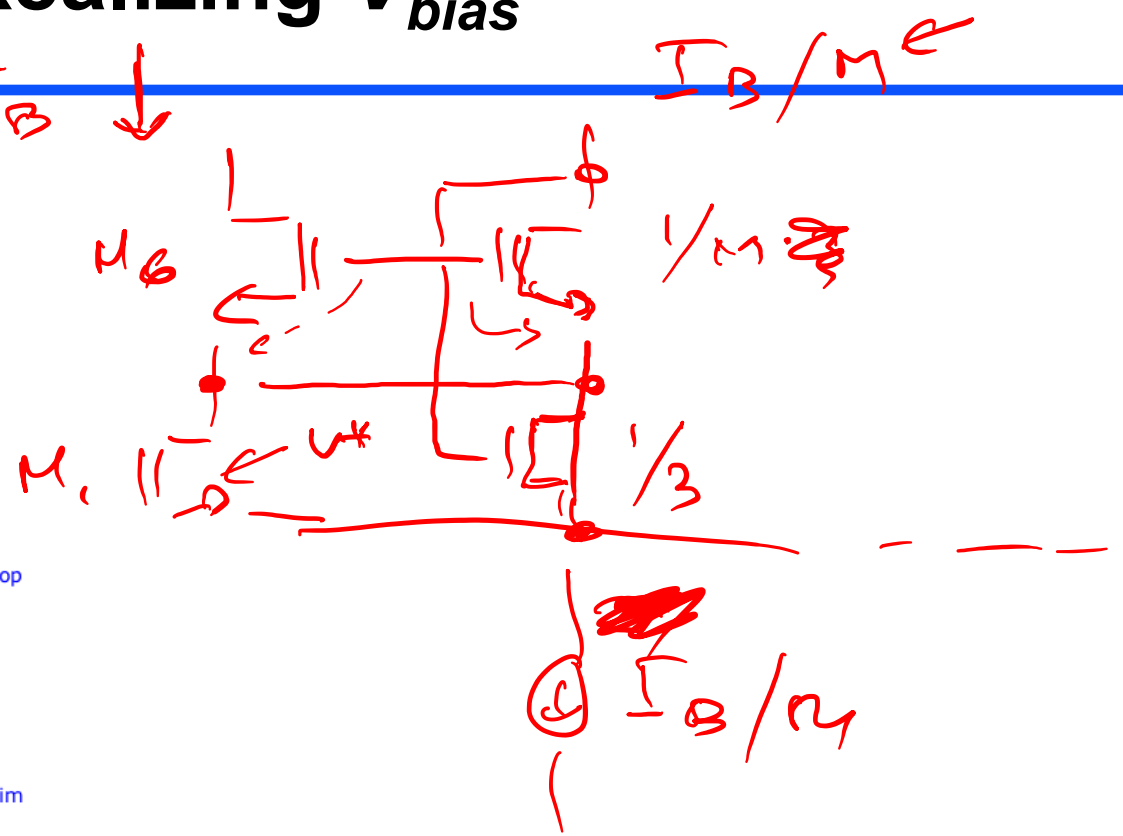
-

$$V_{o,max} = 2 \cdot (V_{DD} - V^*_{1,3,5,6,8,10})$$

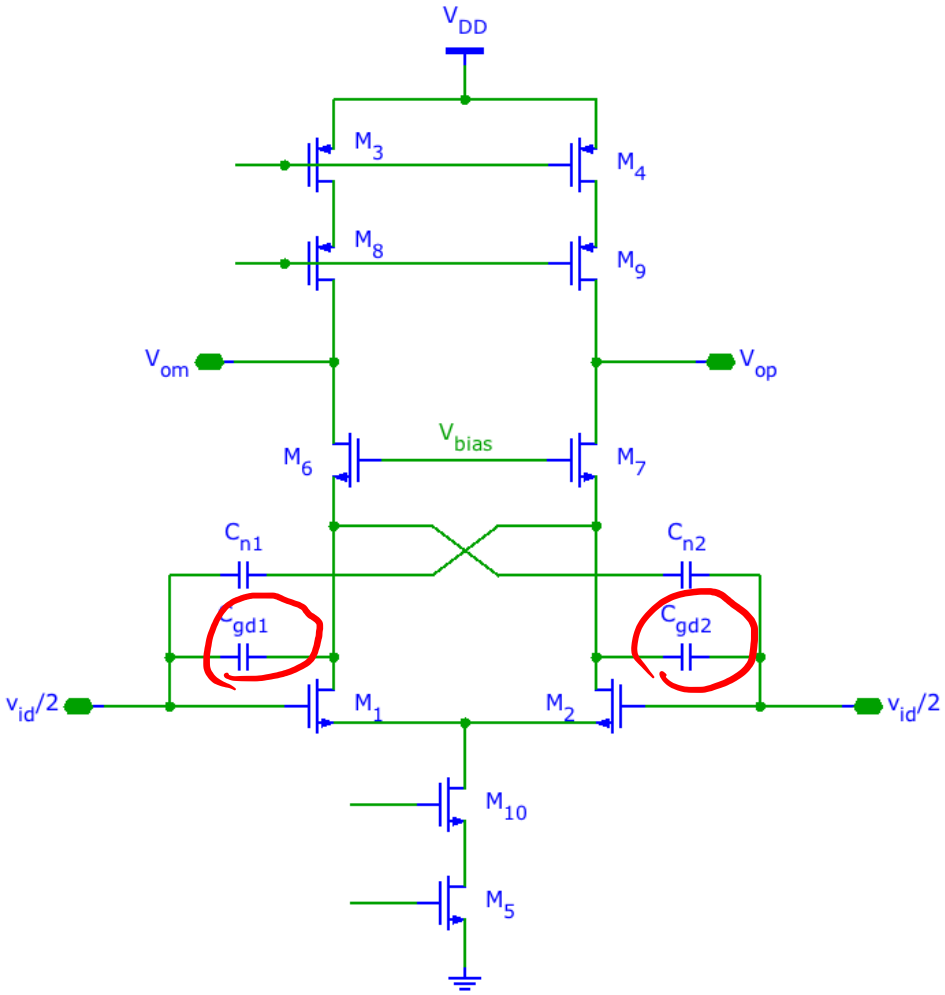
$$\approx 2 \cdot (V_{DD} - 6V^*)$$

Realizing V_{bias}

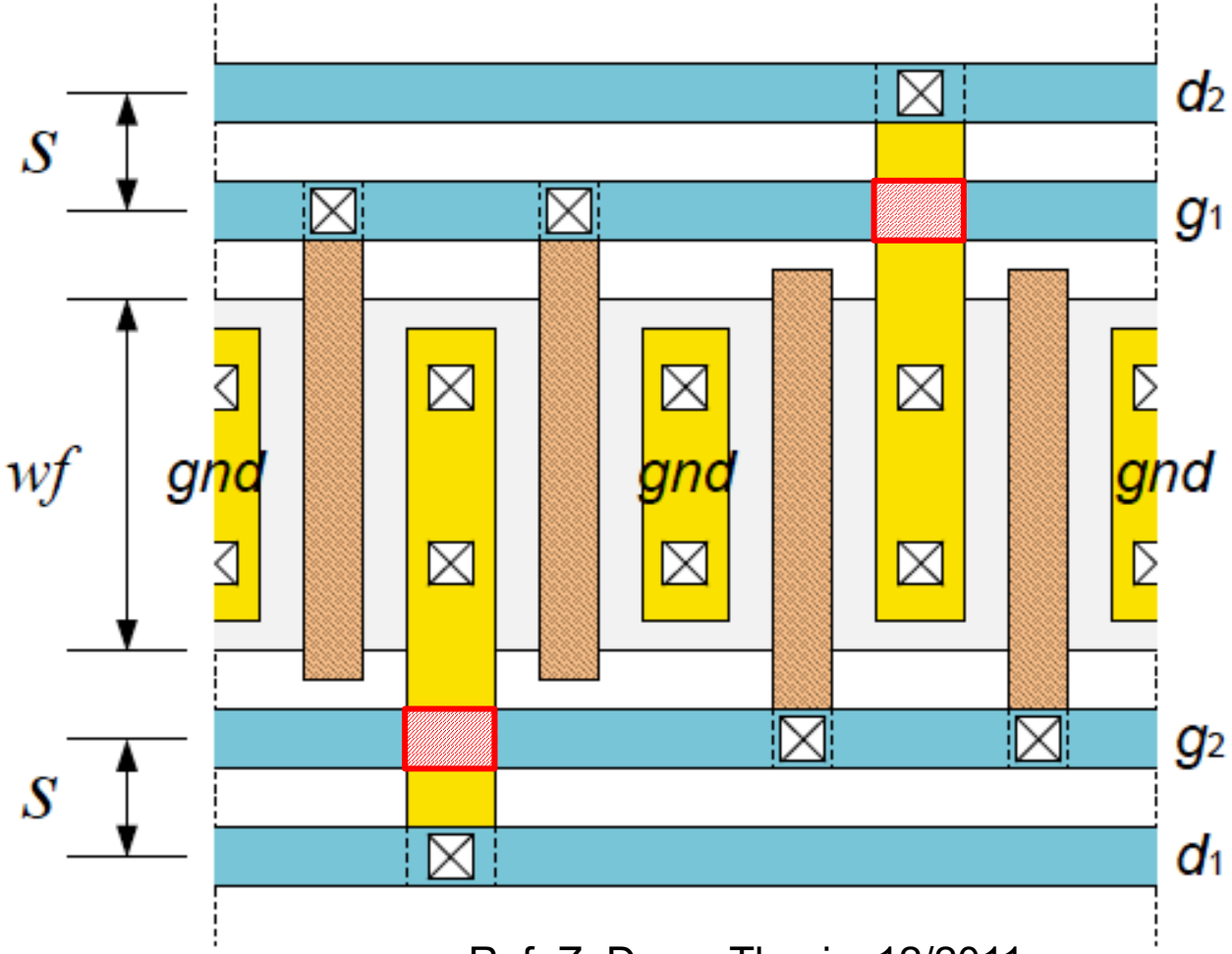




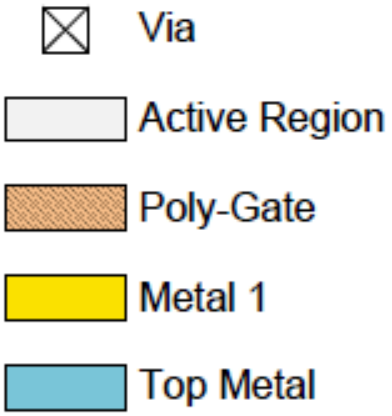
Input Capacitance



Neutralization Capacitor Layout

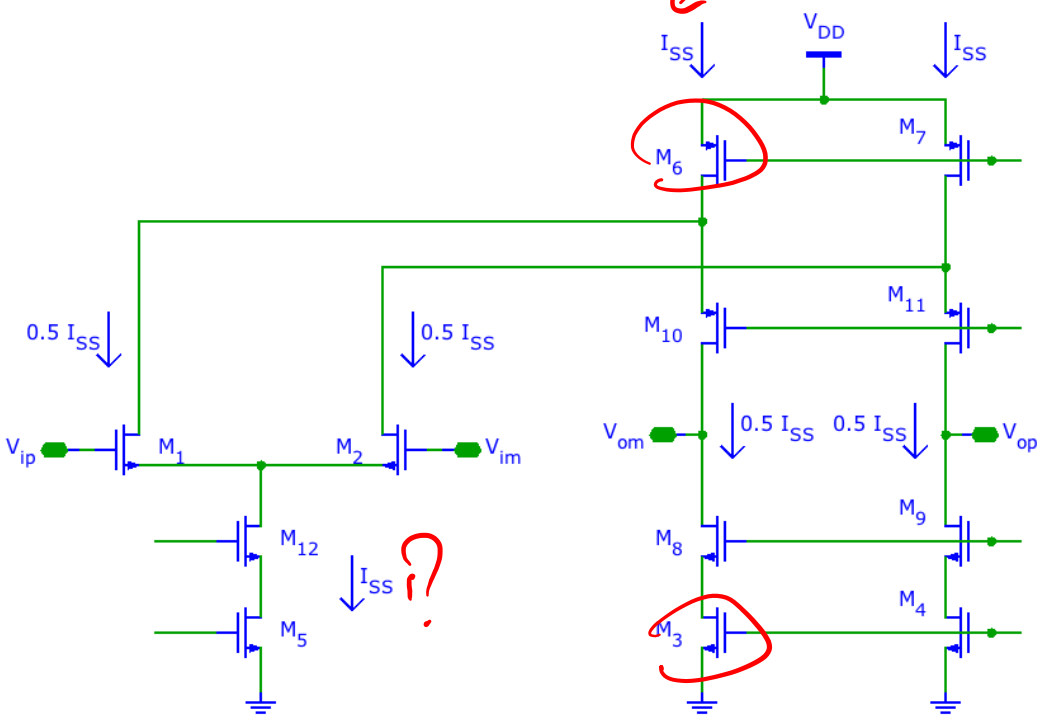


- C_n
- Note that this layout also minimizes wiring C_{gd}
- For high-speed applications



Ref: Z. Deng, Thesis, 12/2011

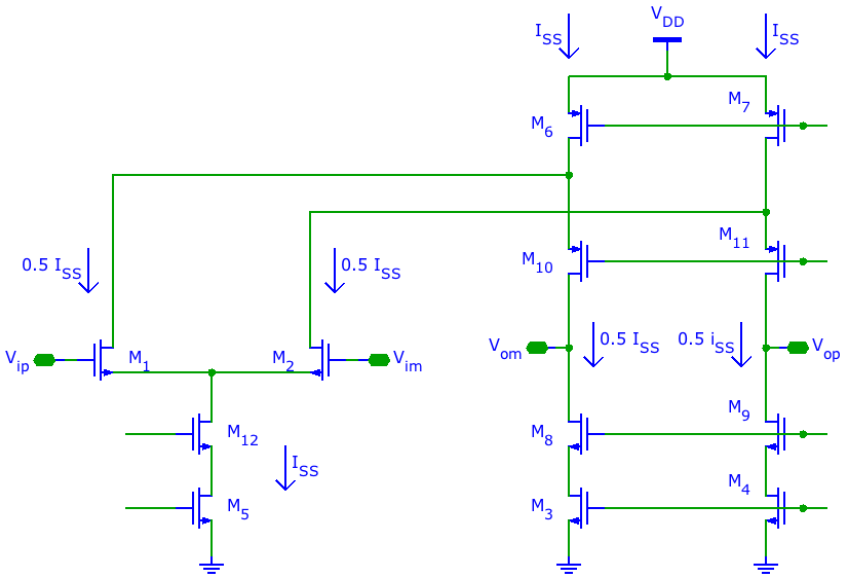
Improved Swing: Folded Cascode

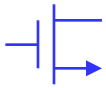


$\overline{i_{on}^2} = 4kT\gamma g_{m1}\alpha_f \left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m6}}{g_{m1}}\right)\left(1 + \frac{V_1^*}{V_3^*} + 2\frac{V_1^*}{V_6^*}\right)$

$\alpha_{cas} \approx 4$

Folded Cascode Noise





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Slewing

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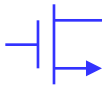
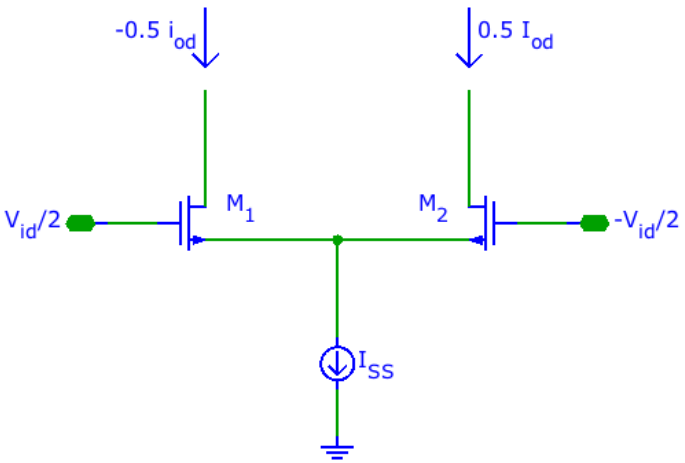
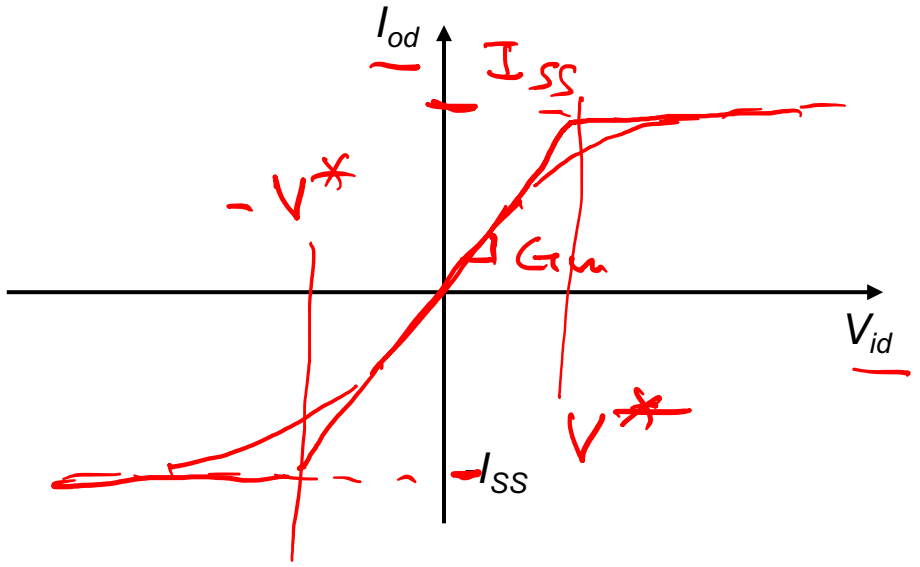


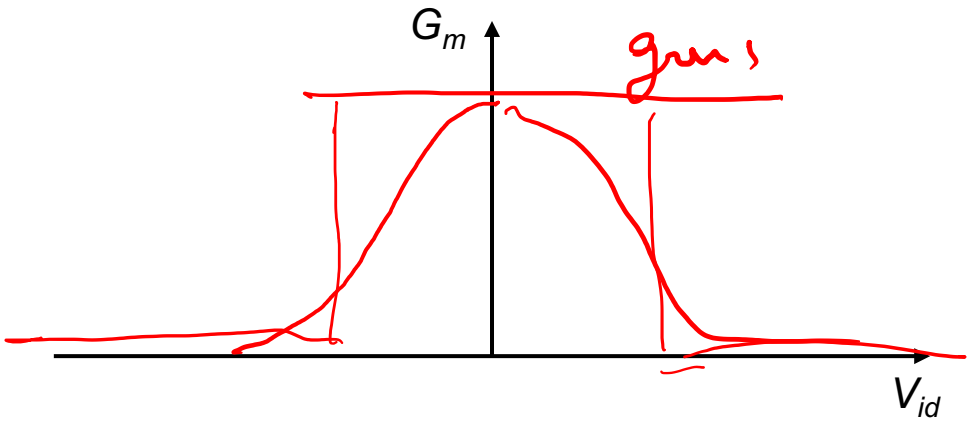
Differential Pair Transconductance





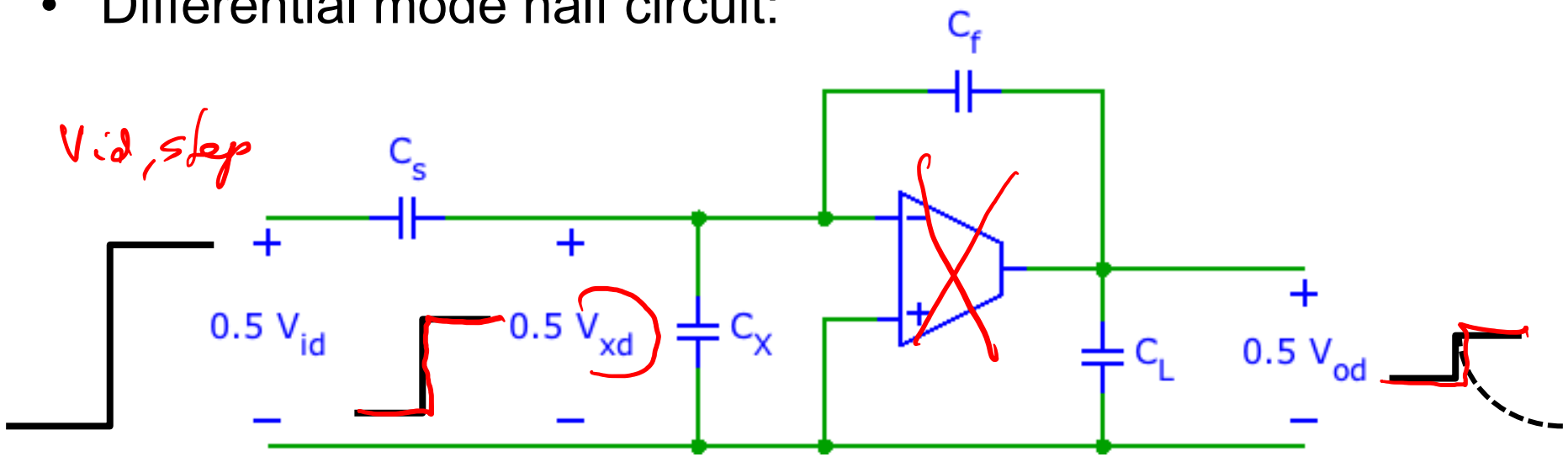
$V_{id} > V^*$

$G_m << g_{m1}$



Initial Transient

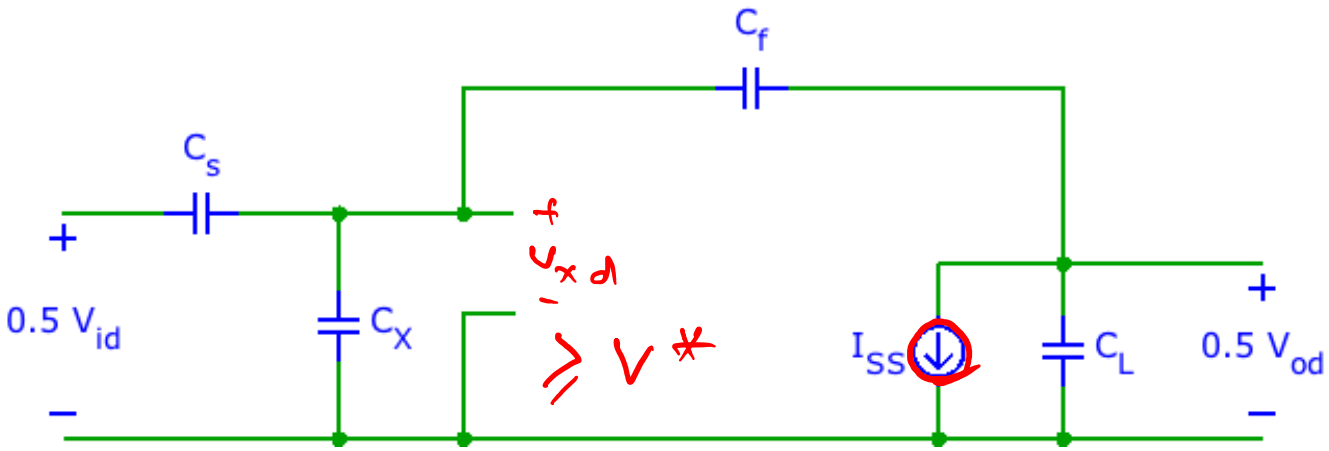
- Differential mode half circuit:



$$V_{xd,step} = V_{id,step} \cdot \frac{C_S}{C_S + C_X + C_L \| C_f}$$

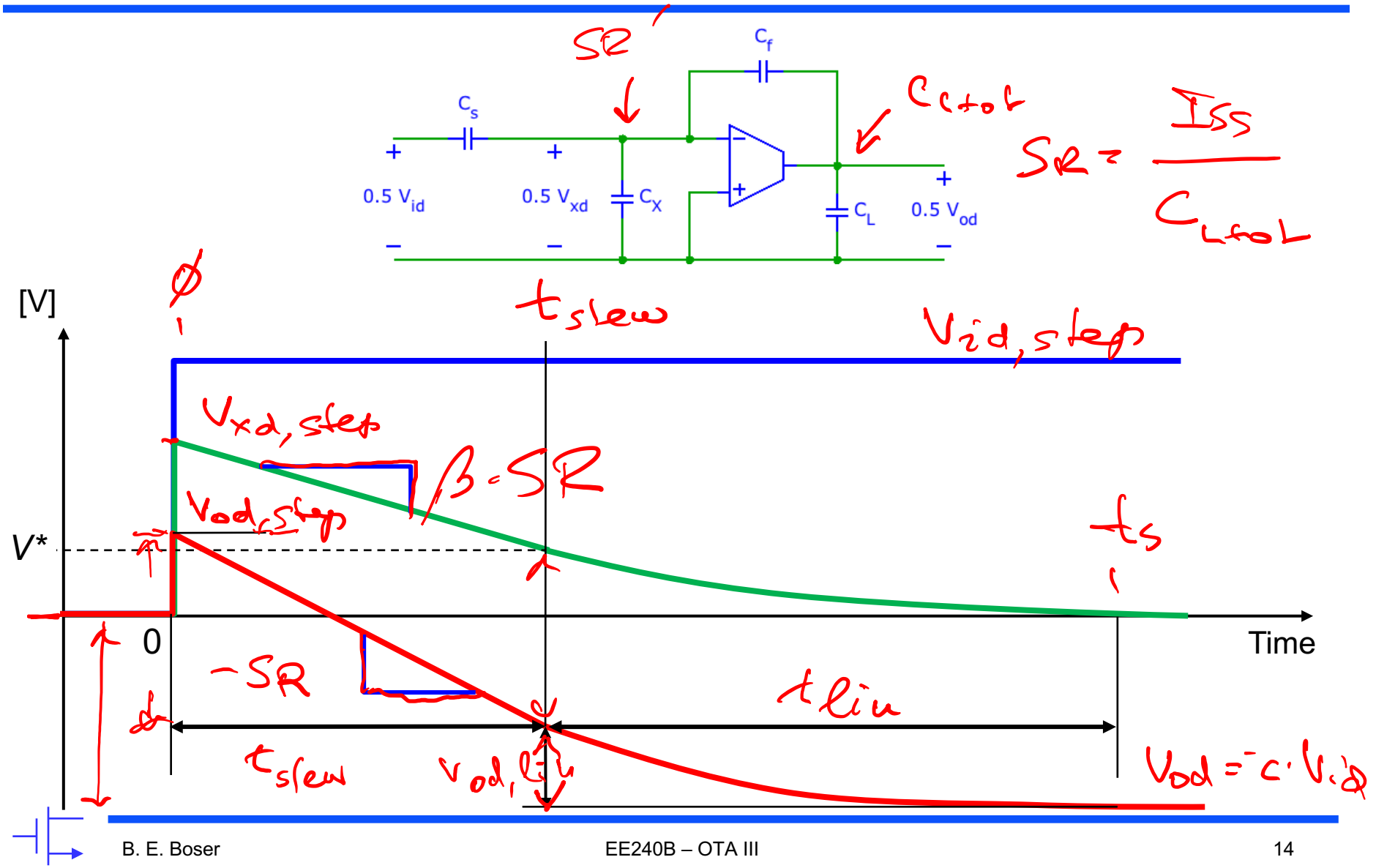
$$\stackrel{?}{>} V^*$$

Circuit Model During Slewing



$$t_{slew} = \frac{|V_{xd,step}| - V^*}{\beta \cdot SR}$$

Initial Transient



Linear Settling

$$|V_{xd}| \leq V^*$$

$$\Rightarrow V_{od,lin} = c \cdot V_{i,d} - V_{od,slew}$$

$$= c \cdot V_{i,d} - t_{slew} \cdot SR$$

$$\therefore t_{lin} = -\tau \cdot \ln\left(\varepsilon_d \cdot \frac{c \cdot V_{i,d}}{V_{od,lin}}\right)$$

~~Area~~ slew settling

Settling Time with Slewing

$$t_s = t_{s,slew} + t_{lin}$$

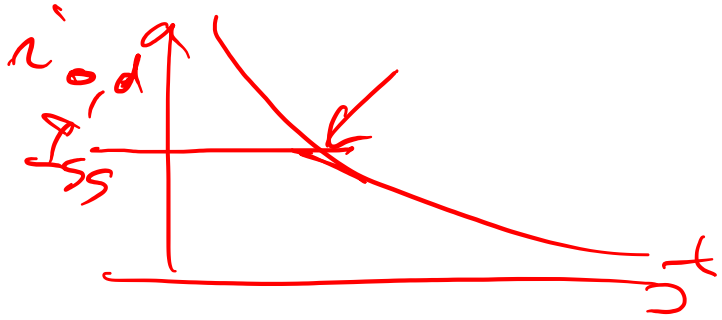
$$\approx \frac{\left| V_{id,step} \cdot \frac{C_s}{C_s + C_x + C_1 \| C_c} \right| - V^*}{\beta \cdot SR} - \tau \cdot \ln\left(\varepsilon_d \cdot \frac{c\, V_{id}}{V_{od,fin}} \right)$$

$V_{xd,step}$

$\frac{V_{od,fin}}{V_{id}} > 1$

Design Procedure with Slewing

- For circuits with significant slewing (large input compared to V^*, small closed-loop gain c)
  1. Start by assuming a slewing time, e.g. 50% of t_s
  2. Design and verify that linear settling completes within t_{lin} (apply only small steps during simulation to avoid slewing)
  3. Now verify with a full-scale input step and check the actual ratio of t_{slew}/t_{lin}
  4. Iterate until the design and verification match
- Typically you get convergence in a few iterations
- Slewing is power efficient
  - Entire bias current used to charge load
  - But limits maximum speed



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Two Stage OTA

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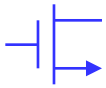
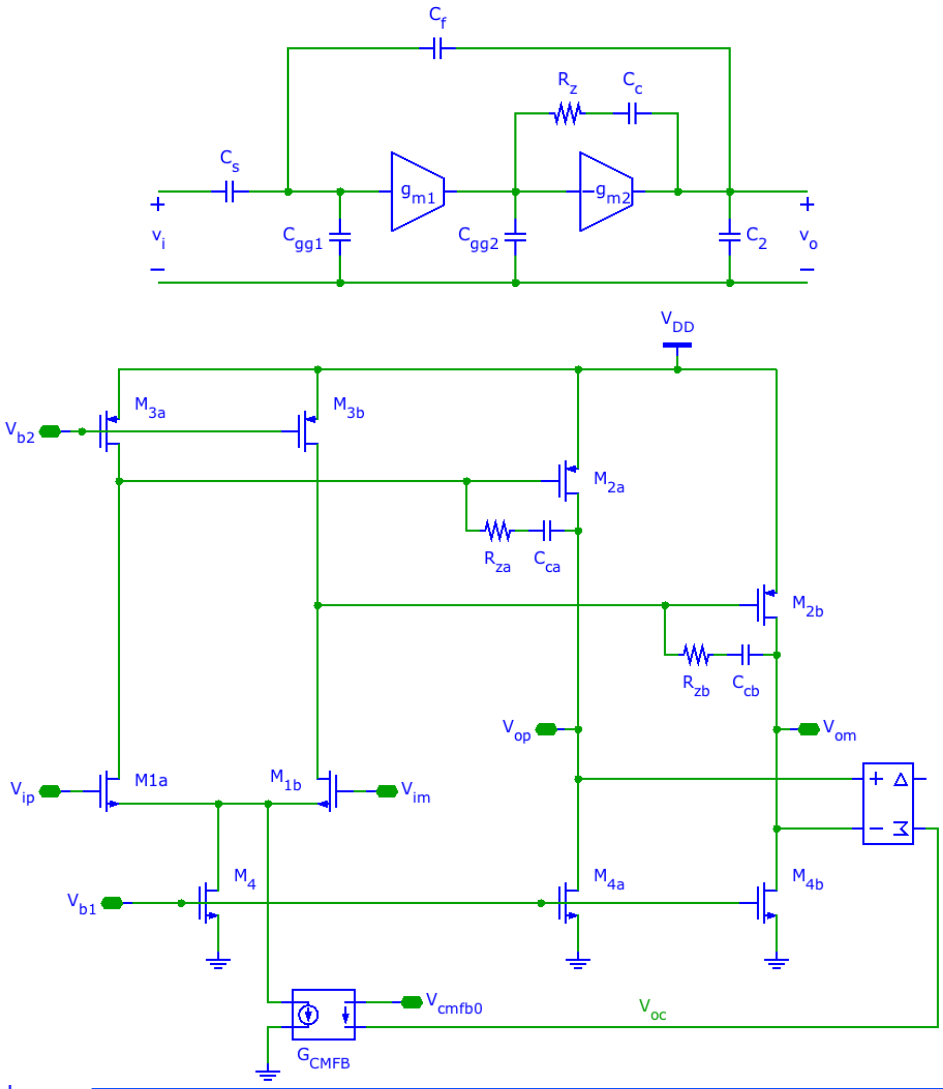
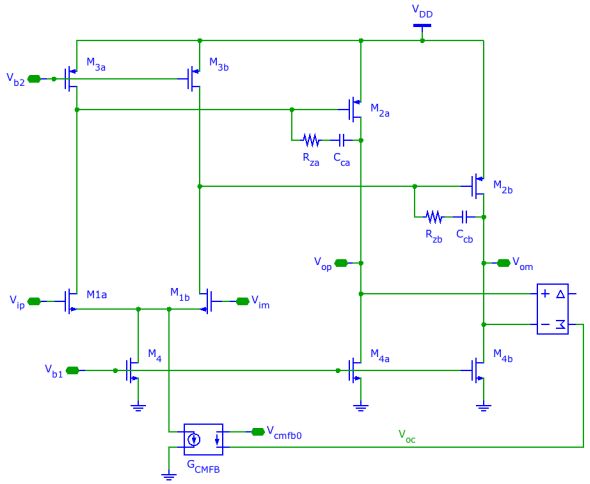
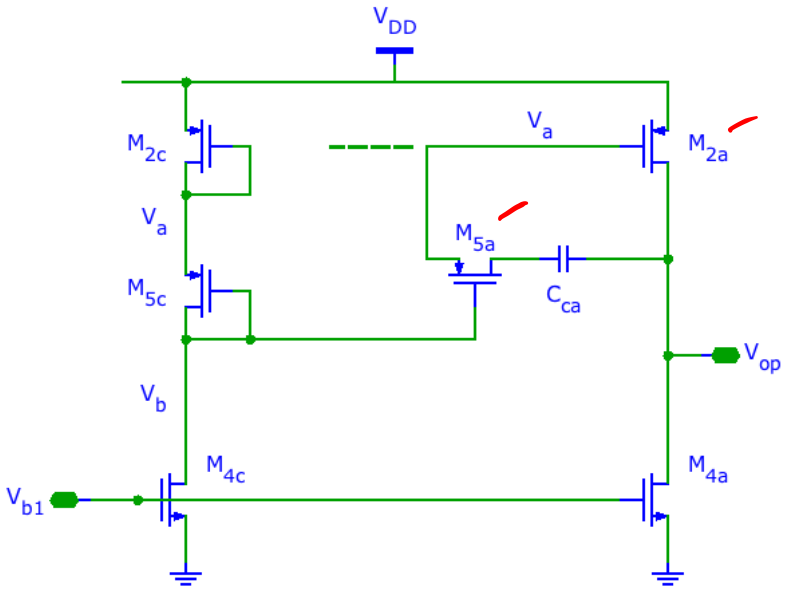


Miller Compensated 2-Stage OTA



Process Insensitive Realization of R_z





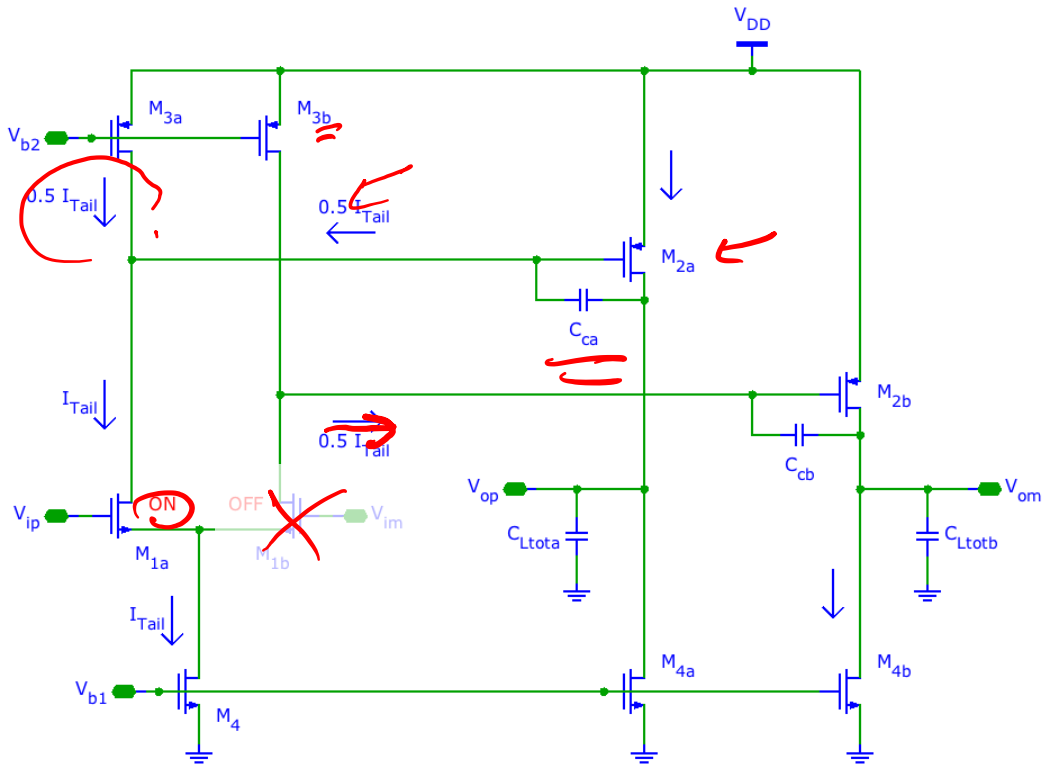
$R_z = \frac{1}{g_{m5a}} = \frac{1}{g_{m2a}}$

M_{2i}, M_{5i}:

- Same I_D
- Same V_{GS}
- Same W/L

$\Rightarrow$ Same g_m !

Slewing in 2-Stage Miller OTA



$SR = \frac{I_{Tail}}{2C_c}$

M_{2a} source

enough current

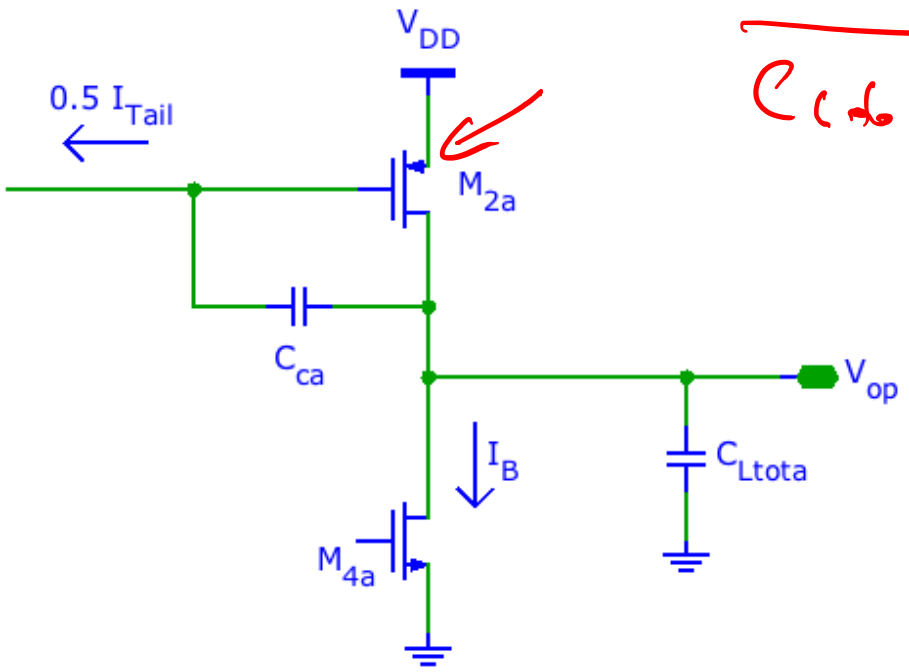
to charge C_{ca}, C_{total}

M_{4a} must sink

...

Ref: M. Yavari et al, "An accurate analysis of slew rate for two-stage CMOS opamps," TCAS-II, March 2005, pp. 164-7.

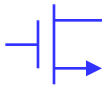
Asymmetric Slewing



$$\frac{I_B}{C_{Ltot} + C_c} \geq \frac{I_{tail}}{2C_c}$$

$$\therefore I_B \geq \frac{I_{tail}}{2} \cdot \left(1 + \frac{C_{Ltot}}{C_c}\right)$$

Why is Symmetric Slewing Important?



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OTA Design Flow

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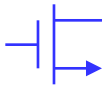
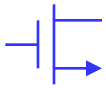


Divide and Conquer Design Flow

- Determine suitable topology based on specifications, e.g.
  - Single or multi-stage
  - Gain boosting
- Script based design
  - Step 1: small-signal
    - Make reasonable assumptions (output range, L, α etc.)
    - Ignore slewing
  - Step 2: large-signal
    - Compute slewing time (use ideal CMFB, biasing), re-optimize
    - Add CMFB, verify stability and settling
      - At this point your design should meet the settling and dynamic range requirements
    - Add biasing, check static settling accuracy
    - Proceed to layout phase: # fingers for transistors, …



Remedies (Examples)

* Excessive Noise
  - Scale
  - A2C caps
  - I_B
  - W
* τ C_{DB}, C_{SB} C_L
* Phase margin

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OTA Examples

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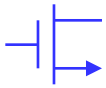
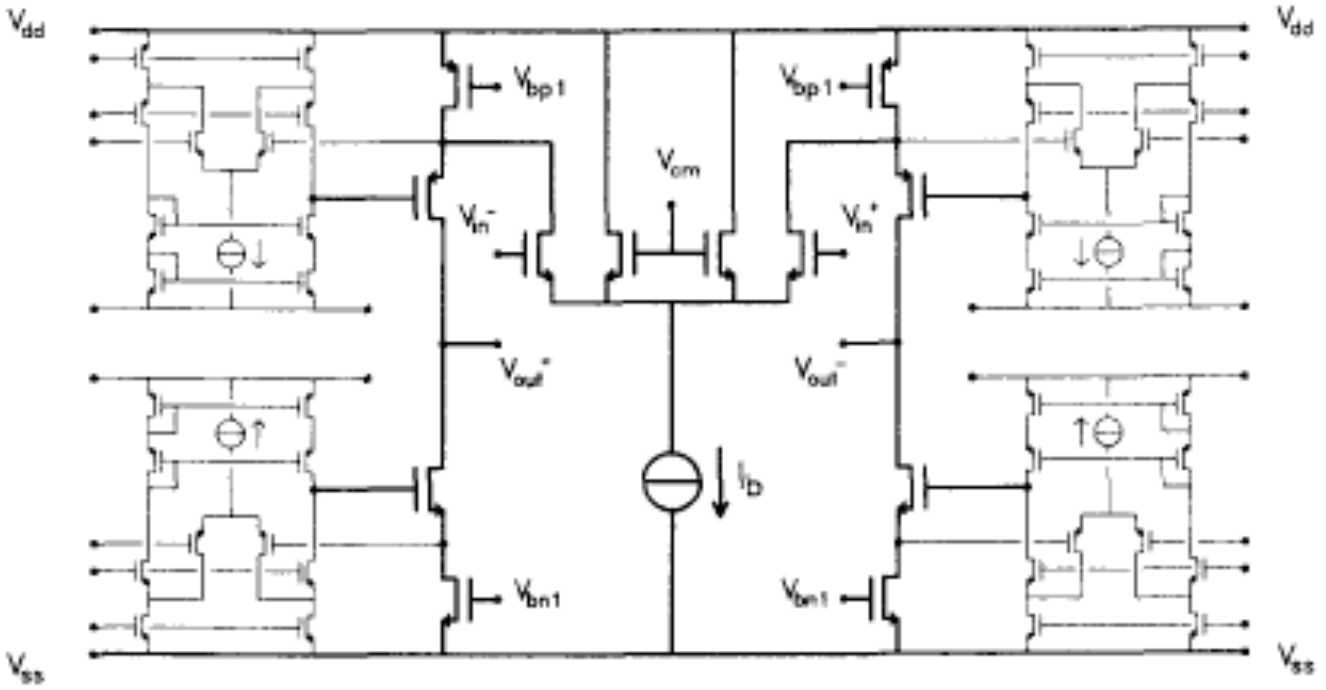
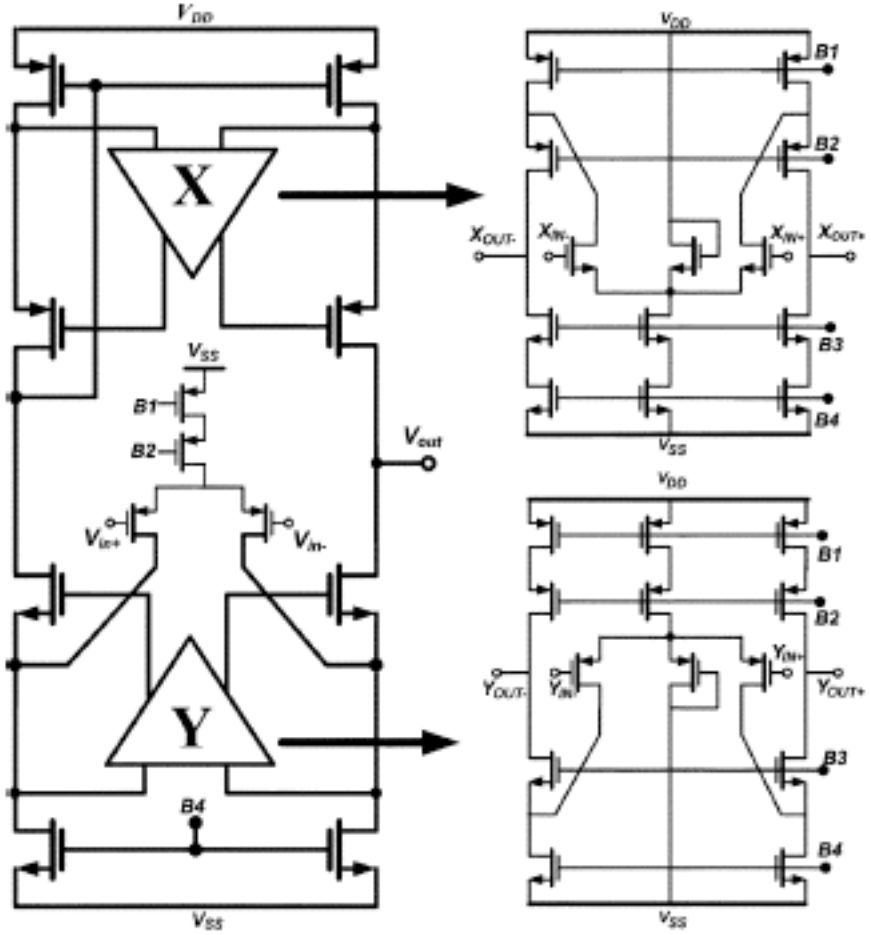


High Gain



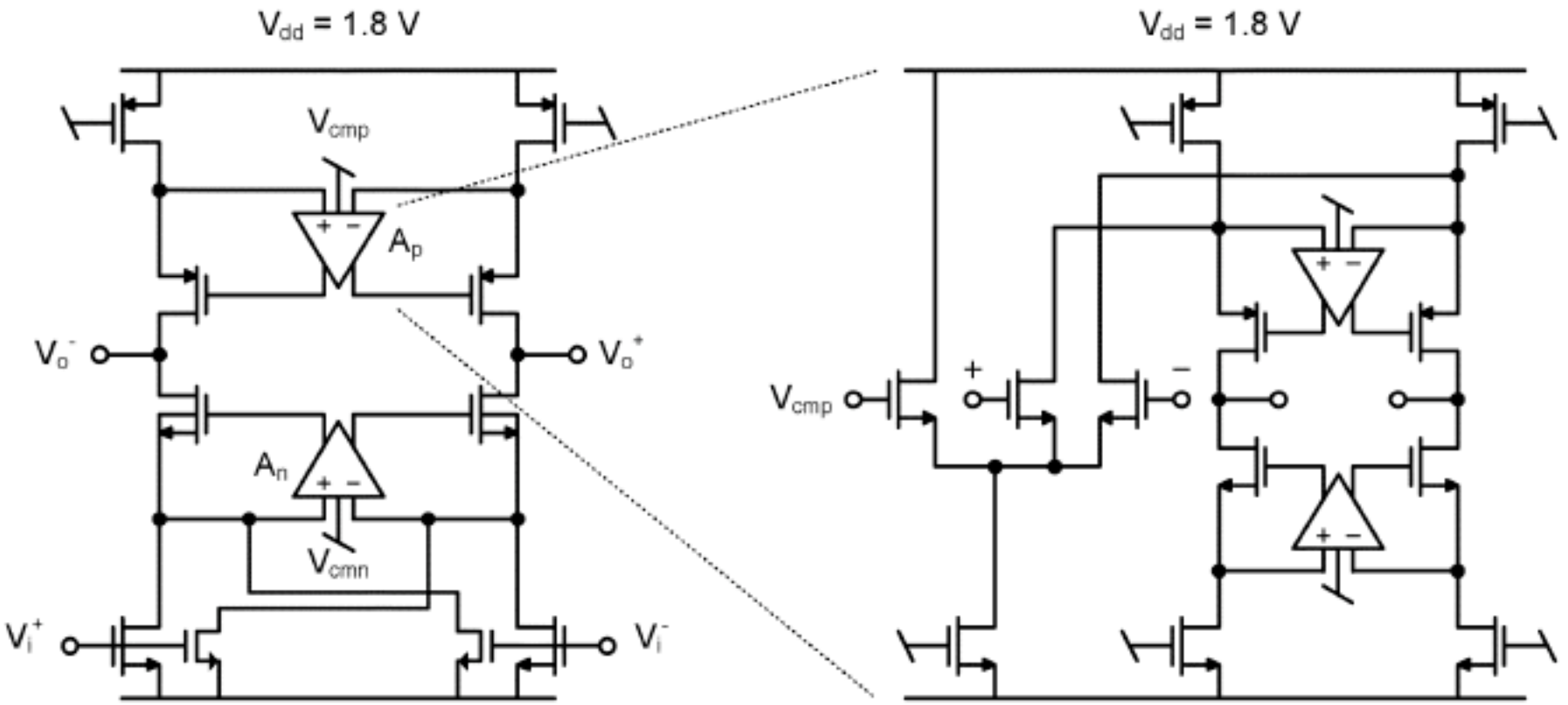
[Bult, JSSC 1992]

Differential Boosters



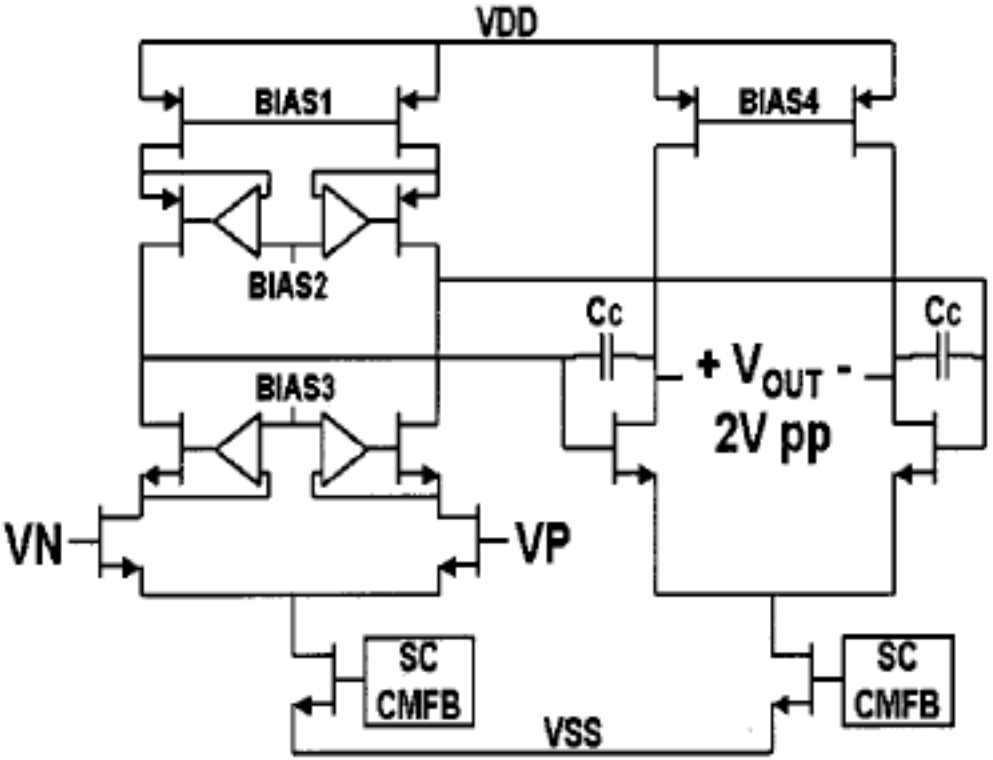
[Ahmadi, TCAS-II, 2006]

Boosted Boosters



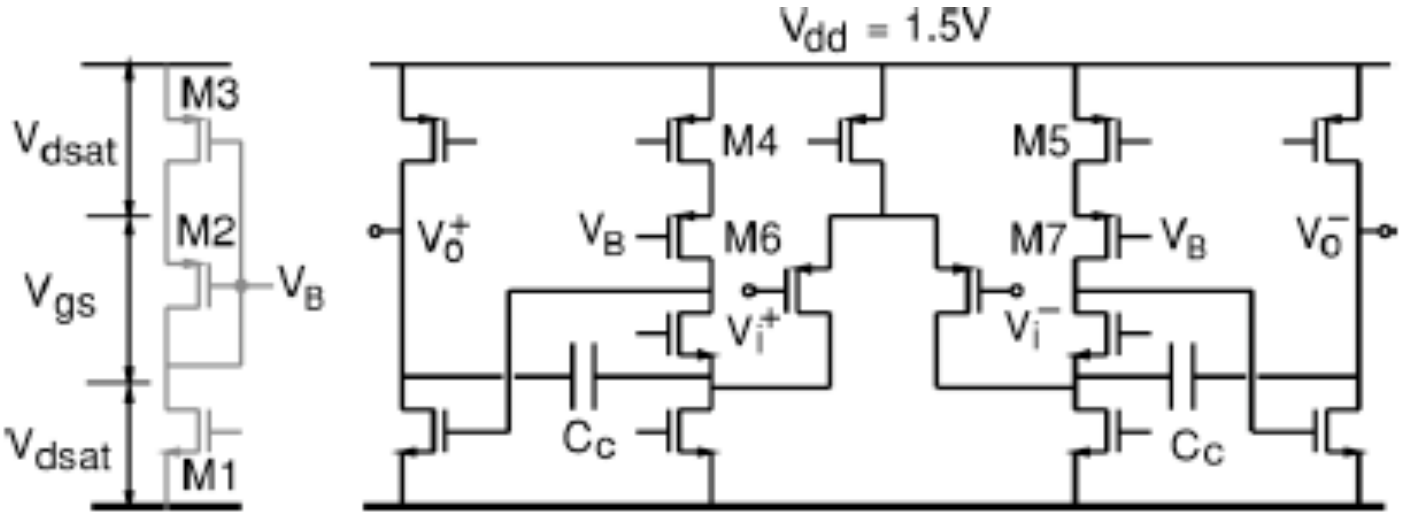
[Chiu, JSSC 2004]

2-Stage OTA with 2 CMFB Loops



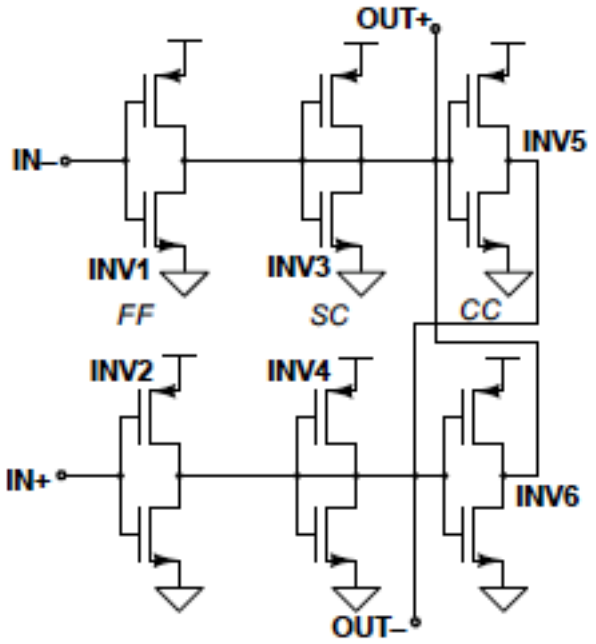
[Yang, JSSC 2001]

2-Stage OTA with Ribner Compensation

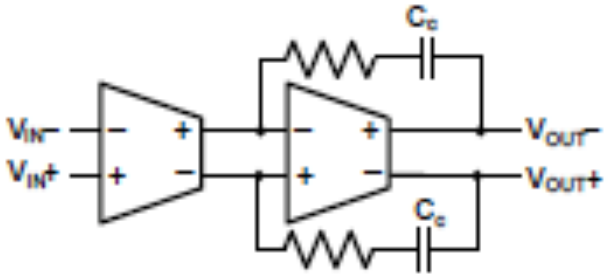


[Abo, JSSC 1999]

Simpler?

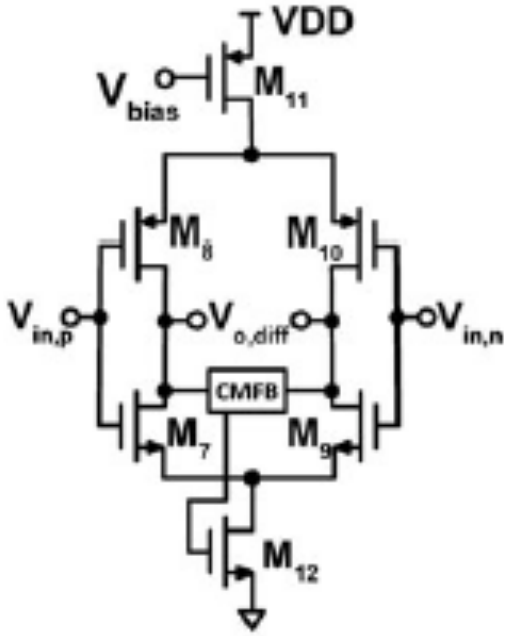


pseudo-differential



[Nauta OTA, Irfansyah, 2014]

Differential & Low Power



Current-starved inverter OTA
(2nd & 3rd integrators)

[Groenen, ISSCC 2016]